AMENDMENTS IN THE CLAIMS

1. (currently amended) An input circuit for providing separate scan and shift paths for a device utilizing single data input latches, said circuit comprising:

a first latch having a single data input port and a single clock input port and an output port;

a second latch also having a single data input port and a single clock input port and an output port;

means for receiving a first clock input signal that enables selection of a scan chain input [[at]] to said first latch and said second latch;

means for receiving a second clock input signal that enables selection of a shift chain input [[at]] to said first latch and said second latch; and

wherein a selection of the scan chain input for passing to said input ports of said latches occurs exclusive of selection of the shift chain input for passing to said input ports, and vice versa, and wherein said single data input latches provide functionality of latches that support multiple inputs.

2. (previously presented) The input circuit of Claim 1, further comprising:

means for receiving said scan chain input; and

means for receiving said shift chain input.

3. (previously presented) The input circuit of Claim 1, further comprising:

means for receiving a data signal at the data input port of each of said latches, wherein said data signal is one of a scan chain input and a shift chain input;

means for accepting the scan chain input into said latches to commence a scan chain operation within said device when the first clock input signal is on; and

means for accepting the shift chain input into said latches to commence a shift chain operation within said device when the second, different clock input signal is on, wherein only one of the first clock input signal and the second, different clock input signal is on at a time and both said scan chain operation and said shift chain operation are supported by said single data input latches.

4. (previously presented) The input circuit of Claim 3, wherein:

said means for accepting the scan chain input includes a first NAND gate that receives as inputs a first clock signal along with a scan chain input and yields a scan chain NAND output;

said means for accepting the shift chain input includes a second NAND gate that receives as inputs a second clock signal along with a shift chain input and yields a shift chain NAND output, wherein both said first and second NAND gates process inputs during an input operation; and

a third NAND gate that receives as input said scan chain NAND output and said shift chain NAND output, wherein both outputs are subsequently NANDed to yield a two-tiered NAND result.

5. (previously presented) The input circuit of Claim 4, further comprising a non-inverting buffer that temporarily delays the two-tiered NAND result prior to forwarding said two-tiered NAND result to the first and second latches as their input, wherein said NAND result is delayed for a pre-set period of time during which a respective clock input signal is on.

6. (previously presented) The input circuit of Claim 1, wherein said second clock input is ANDed with a shift input to yield a shifted second clock input that is utilized as the second clock input for selection of said shift chain input.

7. (previously presented) The input circuit of Claim 1, further comprising an OR gate having inputs of said first clock input signal and a result of an ANDing of said second clock input signal with a shift input, wherein an output of an OR gate is utilized as the clock input of the first and second latches.

8. (previously presented) The input circuit of Claim 1, wherein said first clock input signal and said second clock input signal each provide a select signal for respectively receiving either said scan chain input or said shift chain input into said latches, wherein further, the selected input triggers a respective scan chain or shift chain operation to be completed through the device.

9. (previously presented) The input circuit of Claim 1, wherein said latches are scan-only LSSD latches.

10. (original) The input circuit of Claim 1, wherein said device is a semiconductor device and said input circuit is fabricated on said semiconductor device.

11. (original) The input circuit of Claim [[9]] 10, wherein said semiconductor device is an eFuse device.

12. (previously presented) In a device that includes multiple electrical fuse (eFuse) circuits that are serially connected, a circuit for programming and testing electrical fuses, said circuit comprising:

an input circuit that enables a scan only latch to be utilized to dynamically select from among a scan chain path and a shift chain path being inputted to said device utilizing a series of input clock signals operating as MUX selects for the scan only latch to select either said scan chain path or said shift chain path for passing through said device;

serially connected eFuse circuit comprising:

AND logic having two inputs and an output;

a multiplexer (MUX) having a first input, a second input, a select input, and a MUX output, wherein said output of said AND logic is coupled to said select input of said MUX;

wherein, said eFuse circuit includes a fuse coupled to a switch that is controlled by signals from a fuse latch, a pattern latch, and a program signal source, said pattern latch being programmed with a fuse blow status indicating whether or not said fuse is to be blown during device testing; and

means for connecting components and signals of said eFuse circuit to said MUX and said AND logic, wherein said MUX and said AND logic provide a bypass function that determines when a shifted "1" that is serially passed to each of said eFuse circuits should be forwarded to said fuse latch for initiating a blow of said fuse, wherein when a fuse blow status within said pattern latch indicates that said fuse is not to be blown, said MUX forwards said shifted 1 to a next eFuse circuit without forwarding said shifted 1 to said fuse latch; and

coupling means for connecting said input circuit to said serially connected eFuse circuit such that both a scan chain path and a shift chain path are supported within said device utilizing said scan only latches.

13. (previously presented) The device of Claim 12, wherein:

a first input of said AND logic is coupled to a complement signal of said fuse blow status;

a second input of said AND logic is coupled to said program signal source;

said first input of said MUX is coupled to said fuse latch;

said second input of said MUX is coupled to a MUX output of a previous MUX; and

said MUX output of said MUX is connected to a second input of a next MUX.

14. (previously presented) The device of Claim 13, wherein, said eFuse circuit is a first eFuse circuit and is serially connected to at least a second eFuse circuit whose fuse bow status indicates no blowing of its fuse and a third eFuse circuit whose fuse blow status indicates a blowing of its fuse, said circuit comprising:

means for routing said shifted 1 through said fuse latch of said first eFuse circuit, bypassing a fuse latch of said second eFuse circuit and routing said shifted 1 through a fuse latch of said third eFuse circuit, wherein only said first eFuse circuit and said second eFuse circuit utilizes processing time for routing said shifted 1 through respective fuse latches.

15. (previously presented) In a device that includes a single input, scan-only latch and a two-tiered NAND gate circuit configuration providing a resulting output to said single input latch, and a series of clock inputs, a system for reducing surface area required for supporting both scan chain and shift chain operations within the device, said system comprising:

means for receiving the resulting output at the input port of said latch, wherein said resulting output is one of a scan chain input and a shift chain input;

means for selectively accepting the scan chain input into said latch to commence a scan chain operation within said device only when a first clock input is on; and

means for alternatively accepting the shift chain input into said latch to commence a shift chain operation within said device only when a second, different clock input is on, wherein only

one clock signal is on at a time and both said scan chain operation and said shift chain operation are supported by said single input, scan only latch.

16. (previously presented) The device of Claim 15, wherein:

said means for accepting the scan chain input includes a first two-input NAND gate that receives as input a first clock signal along with a ScanIN input and yields a scan chain NAND output;

said means for accepting a shift chain input includes a second two-input NAND gate that receives as input a second clock signal along with a shiftIN input and yields a shift chain NAND output, wherein both said first and second NAND gates process their respective inputs during an input operation; and

said system further comprises a third NAND gate that receives as input said scan chain NAND output and said shift chain NAND output, wherein both outputs are subsequently NANDed to yield a two-tiered NAND result.

17. (previously presented) The device of Claim 16, wherein said system further comprises a buffer that temporarily delays the two-tiered NAND result prior to sending said two-tiered NAND result to said latch as the input, wherein said two-tiered NAND result is delayed for a preset amount of time corresponding to a time a respective clock input is on.

18. (previously presented) A method for reducing surface area required for supporting both scan chain and shift chain operations within a device that includes a single input scan-only latch and a two-tiered NAND gate circuit configuration providing a resulting output to said single input latch, and a series of clock inputs, said method comprising:

receiving the resulting output at an input port of said latch, wherein said resulting output represents one of a scan chain input and a shift chain input;

accepting the scan chain input into said latch to commence a scan chain operation within said device only when a first clock input is on; and

accepting the shift chain input into said latch to commence a shift chain operation within said device only when a second, different clock input is on, wherein only one clock signal is on at a time and both said scan chain operation and said shift chain operation are supported by said single input, scan only latch.

19. (previously presented) The method of Claim 18, further comprising:

NANDing a first clock input signal with a scanIN input in a first NANDing operation;

NANDing a second clock input signal with a shiftIN input in a second NANDing operation; and

subsequently NANDing a result of said first NANDing operation on said scanIN input and said second NANDing operation on said shiftIN input to yield a two-tiered NAND result.

20. (previously presented) The method of Claim 19, further comprising buffering the two-tiered NAND result prior to sending said two-tiered NAND result to said latch as the inputs, wherein said NAND result is delayed for a preset amount of time corresponding to a time when a respective clock input is on.